Electronic camera with **memory card** interface to a computer
K Parulski, RJ Souvy, TJ Tredwell... - US Patent 5,475,441, 1995 - Google Patents
... provide image data to the computer 10 over the 5 normal PCMCIA data lines, as shown in Table I. The camera includes **memory** which defines the **"card"** as a ... 2A, the camera 20 is shown with an optical system 28, a flash unit 30, a view finder **32**, and a capture **switch** 34. ...
Cited by 180 - Related articles - All 2 versions

Address lookup in packet data communications link, using hashing and content-addressable **memory**
BA Spinney - US Patent 5,414,704, 1995 - Google Patents
... 22, 1992, by Nigel Terence Poole, for "CROSSBAR **SWITCH** FOR SYNTHESISING MULTIPLE BACKPLANE IN- TERCONNECT ... other features and advan- embodiment using 56-**bit** data paths to **memory**), advan- tages ... 1; hashed **address** minus the bottom **16**-**bit** field) in the FIG. ...
Cited by 354 - Related articles - All 2 versions

Data appraisal, evaluation and display for synchrotron radiation experiments: hardware and software
C Boulin, R Kempf, MHJ Koch... - Nuclear Instruments and ..., 1986 - Elsevier
... F & READ IN MA III r5l u in **MEMORY** CHIP 64Kx 1bit **SHIFT** REGISTER DATA (WRITE PIXEL) WRITE a WRITE1 WRITE 2 ... To keep the hardware simple, the **card** only produces a full screen cross-hair cursor generated by comparison of the current pixel ... SWD **switch** the video ...
Cited by 205 - Related articles - All 2 versions

Flashtoaster for reading several types of flash-**memory cards** with or without a PC
LL Jones, S Mambakkam... - US Patent 6,438,638, 2002 - Google Patents
... GDI 27 DII — — — 28 D12 — — — 29 D13 — — — 30 D14 — — — 31 D15 — — — **32** -CE2 — — — 33 ... 98 90 GP-IO 99 40 **USB** FACE 100 CLK DATA **16-BIT** FIG. 10 ... **US** 6,438,638 BI FLASHTOASTER FOR READING **SEVERAL** TYPES OF FLASH-**MEMORY CARDS** WITH OR ...
Cited by 145 - Related articles - All 2 versions

Field programmable port extender (FPX) for distributed routing and queuing [PDF] from psu.edu
JW Lockwood, JS Turner... - Proceedings of the 2000 ACM ..., 2000 - portal.acm.org
... For line **cards** that operate at OC3 rates (155 Mbits/sec- ond), each **memory** provides 53 * 8/155M ... The result of the lookup is used by the WUGS **switch** to deliver the packet to the appropriate ... The **32-bit** data path width and 4 clock cycle latency of the **memory** suggest an optimal ...
Cited by 35 - Related articles - All 25 versions

Control processor switchover for a telecommunications **switch**
MN Ganmukhi, RL Baracka Jr, MP DeMilia... - US Patent ..., 1999 - Google Patents
... **card** also includes an FPGA based control pro- cessor Utopia Adapter 112 with a bidirectional single ATM cell deep FIFO **memory** to match a ... EMBus 130 of control processor WRITE cycle concludes with **SXRDY_L** asserted followed **card** 12 connects to **switch** fabric **16** ...
Cited by 76 - Related articles - All 2 versions

Intelligent power supply system for a portable computer
H Shimamoto... - US Patent 5,300,874, 1994 - Google Patents
... "Linear supplies are inefficient compared wtih **switch**- ing supplies ... A bus driver (BUS-DRV) **16** serves as ... An 15 connected via the **I/O** register 301 and internal bus 307 extension **memory card** (EXTM) 30 is arbitrarily con- to ^ pc-**CPU** 306, selectively controls the battery in nected ...
Cited by 178 - Related articles - All 2 versions

AMBA: enabling reusable on-chip designs [PDF] from umich.edu
D Flynn - Micro, IEEE, 1997 - ieeexplore.ieee.org
... External static **memory** emulation bank. The bank is 512 Kbytes, user-programmable, and split into two banks of emulated **SRAM** or ROM, each with DIP **switch** configuration of **32**-, **16**-, and 8-**bit**-wide **memory** with one to four wait states. ... CPU daughter **card**. ...
Cited by 131 - Related articles - BL Direct - All 7 versions

The MIPS R10000 superscalar microprocessor [PDF] from toronto.edu
KC Yeager - Micro, IEEE, 1996 - ieeexplore.ieee.org
... A load or store instruction may need to be retried if it has a **memory address** dependency or misses in the data cache. Two **16**-bitxlb-**bit** matrixes track dependencies between **memory** accesses. The rows and columns correspond to the queue's entries. ...
Cited by 746 - Related articles - BL Direct - All 42 versions

Address transition detection sensing interface for flash **memory** having multi-**bit** cells
A Bashir - US Patent 5,594,691, 1997 - Google Patents
... Static **memory 16** may include a flash electrically erasable programmable read-only **memory** ("flash EEPROM") or ... 17 may be a solid state hard drive 17 using multiple **bit** per cell ... in the computer system and are coupled to a Personal Computer **Memory Card** Industry Association ...
Cited by 76 - Related articles - All 2 versions

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